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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/054,933	04/03/1998	CRAIG R. FRINK .	A0521/7153	3289	
26643 75	26643 7590 09/22/2004			EXAMINER	
PETER J. GORDON, PATENT COUNSEL			BUI, KIEU OANH T		
AVID TECHNOLOGY, INC. ONE PARK WEST TEWKSBURY, MA 01876			ART UNIT	PAPER NUMBER	
			2611	15	
			DATE MAILED: 00/22/200/		

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)			
· ·	09/054,933	FRINK, CRAIG R.			
Office Action Summary	Examiner	Art Unit			
•					
The MAILING DATE of this communication	KIEU-OANH T BUI	t with the correspondence address			
Period for Reply	ruppears on are cover since	t with the correspondence address -			
A SHORTENED STATUTORY PERIOD FOR RITHE MAILING DATE OF THIS COMMUNICATION Extensions of time may be available under the provisions of 37 Clafter SIX (6) MONTHS from the mailing date of this communication of the period for reply specified above is less than thirty (30) days, of If NO period for reply is specified above, the maximum statutory properties of the period for reply within the set or extended period for reply will, by any reply received by the Office later than three months after the earned patent term adjustment. See 37 CFR 1.704(b).	ON. FR 1.136(a). In no event, however, main. a reply within the statutory minimum of eriod will apply and will expire SIX (6) I statute, cause the application to becom	y a reply be timely filed f thirty (30) days will be considered timely. MONTHS from the mailing date of this communication. e ABANDONED (35 U.S.C. § 133).			
Status 					
1) Responsive to communication(s) filed on <u>06 October 2003</u> .					
2a) This action is FINAL . 2b) This action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice und	der <i>Ex par</i> te <i>Quayle</i> , 1935 (C.D. 11, 453 O.G. 213.			
Disposition of Claims					
4)⊠ Claim(s) <u>1-4,9 and 11</u> is/are pending in the	e application.				
4a) Of the above claim(s) is/are withdrawn from consideration.					
5) Claim(s) is/are allowed.					
6)⊠ Claim(s) <u>1-4, 9, and 11</u> is/are rejected.					
7) Claim(s) is/are objected to.					
8) Claim(s) are subject to restriction a	nd/or election requirement.	-·			
Application Papers	•	•			
9)☐ The specification is objected to by the Exa	miner				
10) The drawing(s) filed on is/are: a)		to by the Examiner			
Applicant may not request that any objection to					
Replacement drawing sheet(s) including the co	- ' '	• • • • • • • • • • • • • • • • • • • •			
11) The oath or declaration is objected to by th					
Priority under 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for for	eign priority under 35 U.S.C	C. § 119(a)-(ḍ) or (f).			
a) All b) Some * c) None of:					
1. Certified copies of the priority docum		A 11 11 A			
2. Certified copies of the priority docum					
 Copies of the certified copies of the application from the International But 		en received in this National Stage			
* See the attached detailed Office action for a		not received			
212 and disserted detailed emoc detail for a	i not or the contined copies i	iot i cocived.			
Attachment(s)					
1) Notice of References Cited (PTO-892)	4) Intervie	ew Summary (PTO-413)			
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper I	No(s)/Mail Date			
Information Disclosure Statement(s) (PTO-1449 or PTO/SI Paper No(s)/Mail Date	3/08) 5) ☐ Notice 6) ☐ Other:	of Informal Patent Application (PTO-152)			
.S. Patent and Trademark Office					
PTOL-326 (Rev. 1-04) Offic	ce Action Summary	Part of Paper No./Mail Date 20040913			

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DETAILED ACTION

Remarks

1. Applicant's arguments with respect to claims 1-4, 9, and 11 have been considered but are moot in view of the new ground(s) of rejection and the Examiner's argument below. Claims 5-8 and 10 were canceled in the previous amendments papers 12 & 14.

Claim Rejections - 35 USC § 102

- 2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
 - A person shall be entitled to a patent unless (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 3. Claims 1-4, 9, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Munson et al. (US Patent 5,760,794).

Regarding claim 1, Munson discloses "an output interface for a sender of video data, comprising a first output for providing data, and a second output for providing a valid data signal associated with the data output by the first output and indicating whether the output data includes valid video data; a third output for providing a valid command signal indicating whether the data output by the first output includes command data; and wherein the command data includes a memory address at a receiver, wherein the first, second, and third outputs are in parallel; wherein, in response to a request signal received from the receiver, the output interface transfers

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one of valid video data and command data and asserts one of the valid data signal and the valid command signal to the receiver", i.e., Munson discloses an interconnection for video processing using a Direct Memory Access (DMA) controller 106, and DMA Arbiter 107 within entity 100 acting as an output interface, a PCI memory as a sender for providing output data, valid data signal to a receiver such as a graphics memory 113 (Fig. 4) via a PCI interface 109 and PCI bus 115, and the step of verifying a valid video data and a valid command data as the inclusion of memory address within the command data at the receiver in response to a request signal, i.e., DMA request signal, received from the receiver (see Figs. 4 & 16, and col. 5/line 55 to col. 6/line 13; col. 16/line 47 to col. 17/line 6; col. 19/lines 15-60; and col. 27/lines 25-58 for a linked list of commands in order to understand more the operation of data transferring among the DMA controller to either a PCI memory or a graphic memory with memory addresses concerned). In addition, these output signals are in parallel because as Figure 13 and 16 shows a Windows Manager 801 gathers information from memory 111 including windows handle list 804 regarding as command data signals for providing tasks to the Windows Manager in a parallel manner before transferring application data including video and valid data to Graphics Memory 113 for video processing and displaying them to the CRT 112 for the user (col. 26/lines 10-59 and col. 27/lines 10-58).

Regarding claim 2, Munson discloses "an input interface for a receiver of video data, comprising a first input for receiving data, a second input for receiving a valid data signal associated with the data received by the first input and indicating whether the received data includes valid video data; and a third input for receiving a valid command signal indicating whether the data received by the first input includes command data; wherein the command data

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includes a memory address at the receiver, wherein the first, second, and third inputs are in parallel; wherein the input interface stores command data received by the first input in memory of the receiver; and wherein the input interface transfer video data received to the memory address specified in the command data in the memory of the receiver", i.e., i.e., Munson discloses an interconnection for video processing using a Direct Memory Access (DMA) controller 106, and DMA Arbiter 107 within entity 100 acting as an output interface, PCI memory 111 as a sender for providing output data, valid data signal to a receiver such as a graphics memory 113 (Fig. 4) via a PCI interface 109, PCI bus 115 and Graphics I/F 114, and the step of verifying a valid video data and a valid command data as well as the inclusion of memory address within the command data at the receiver in response to a request signal, i.e., DMA request signal, received from the receiver (see Figs. 4 & 16, and col. 5/line 55 to col. 6/line 13; col. 16/line 47 to col. 17/line 6; col. 19/lines 15-60; and col. 27/lines 25-58 for a linked list of commands in order to understand more the operation of data transferring among the DMA controller to either a PCI memory or a graphic memory with memory addresses concerned). In addition, these output signals are in parallel because as Figure 13 and 16 shows a Windows Manager 801 gathers information from memory 111 including windows handle list 804 regarding as command data signals for providing tasks to the Windows Manager in a parallel manner before transferring application data including video and valid data to Graphics Memory 113 for video processing and displaying them to the CRT 112 for the user (col. 26/lines 10-59 and col. 27/lines 10-58). Within this claim, the graphics memory 113 and graphics I/F 114 (Fig. 4) acts as a receiver and an input interface for receiving outputs as noted from the sender or PCI

memory 111; and the process is same as in claim 1, yet the outputs are received at the receiver 113 now instead.

As for claim 3, claim 3 is for a device for sending video data to a memory in another device with a combined limitation from claims 1 and 2 is rejected for the reasons given in the scope of claims 1 and 2 as already discussed in details above.

As for claim 4, in further view of claim 3 above, Munson discloses a memory (Fig. 4/111 & 113) and an input interface and its corresponding features cited above as wherein the input of the input interface further receives a valid command signal indicating whether the data includes command data, wherein the command data includes a memory address in the memory of the device, wherein the input interface transfers valid data received to the memory address specified in the command data in the memory of the device (see Examiner's discussion in claim 2 above).

Claims 5-8 were cancelled.

As for claims 9 and 11, Munson discloses "a device for receiving video data from another device" with its input interface and its output interface; and its "output interface wherein the output interface transfers data to the other device in response to a request signal received from the other device" (see Examiner's discussion in claims 1-4 above).

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Response to Arguments

4. Applicant's arguments filed on 09/02/03 have been fully considered but they are not persuasive.

Applicant simply argues that Munson merely appear to use PCI interface protocol for communication messages regarding data transfer, but then applicant cancels most the pending claims and revises the claim languages of claims 1-4, 9, and 11 for making them appear to be a little more complex and different than the teaching of Munson's reference. However, referring back to pages 5-6 of the present application, this application is simply claiming for a known process of data transfer between a sender device such as a disk controller to a receiver device such as a video processing board via a PCI bus interface. By looking at Munson's Figs. 4, 13, and 16 and its corresponding paragraphs, one of ordinary skill of the art can easily realize that Munson's reference reads on each and every limitation therein for data transfer process between a PCI memory (as a sender) and Graphics Memory 113 (as a receiver) using input interface 100 and PCI bus 115 for data and video communication.

Therefore, the Examiner disagrees with the Applicant's argument and stands with the disclosure and teaching of Munson as previously disclosed in the office action and revised with discussion in this Final office action.

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Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306, (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II. 2121 Crystal Drive, Artington. VII. Cixth Floor (Receptionis).

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7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Krista Kieu-Oanh Bui whose telephone number is (703) 305-0095. The examiner can normally be reached on Monday-Friday from 9:00 AM to 6:00 PM, with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christopher Grant, can be reached on (703) 305-4755.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Krista Bui Art Unit 2611 September 14, 2004 KRISTA BUI PATENT EXAMINER

J. Kumll